A Broadband Upconverter IC

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1.0 Abstract

This paper describes the design and performance of a single-chip upconverter IC consisting of a doubly balanced dual-gate FET mixer, a four-stage LO amplifier, and a single-stage IF amplifier. It converts a dc-to-5 GHz input to an 8-to-10 GHz IF. State-of-the-art performance was achieved through the use of advanced models and circuit-design techniques.

2.0 Introduction

This paper describes the design and performance of a broadband microwave monolithic integrated circuit (MMIC) intended for use as a wide-dynamic-range upconverter. The upconverter consists of a four-stage LO amplifier, a broadband doubly balanced dual-gate FET mixer, and a highly linear IF amplifier integrated on a single chip. Due to a novel mixer topology, the input passband of the converter extends from dc to 5 GHz, the LO frequency range is 8 GHz to 16 GHz, and the IF output frequency range is 8 to 10 GHz.

Figure 1 shows a block diagram of the upconverter IC. The primary design goals for this upconverter were a high third-order intermodulation intercept point (IP_3) and good spurious-response rejection. These were achieved through the use of a dual-gate FET ring mixer, high LO power provided by on-chip amplifiers, and a balanced IF amplifier using relatively large, 600-μm wide devices. Advanced FET models were used to optimize the circuit's intercept points. The converter exhibited an IP_3 of 23.5 dBm across most of the band; second-order intercept points (IP_2) for spurious responses were greater than +40 dBm.

There are many benefits in integrating multiple RF function blocks into a single IC. These include the following: (1) size is reduced significantly over connectorized hybrids; (2) device screening can be performed at the wafer

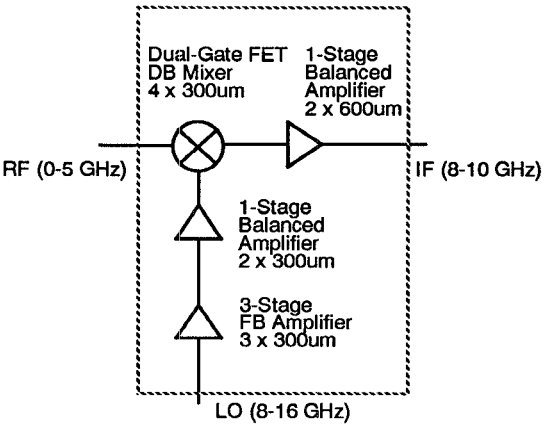

Figure 1. Block diagram of the broadband upconverter IC.

3.0 Components

3.1 Mixer

The goal for the mixer was to develop a planar MMIC circuit having intermodulation and spurious-response performance equivalent to, or better than, hybrid diode mixers. It was necessary to use our standard 0.5 μm MESFET process so that the mixer could be integrated with the amplifier circuits onto a single chip.

The mixer's circuit is shown in Figure 2. This mixer is similar in many respects to some describe elsewhere [1]. It consists of four 300-μm dual-gate FETs in a doubly-balanced configuration; this configuration provides good even-order intermodulation rejection. Unlike most doubly balanced FET mixers, one side of the RF input port is terminated by a 50-ohm resistor, and a current source is included in series with the FETs' sources. This current source eliminates the need for an input balun by creating a differential current in the two arms of the mixer; as one side of the RF input is driven positive, the other must go

negative to keep the current constant. This creates a broadband balun action, even though only one side of the input is driven. The circuit has provisions for bypassing the termination, so an external 0-to-180 degree balun may still be used on the mixer's input; in this configuration, the current source will enhance the even-order spurious-response suppression of the input balun.

Figure 3 shows a schematic representation of the LO and IF baluns. Each balun consists of a Wilkinson power divider followed by a pair of Lange couplers. The unused ports of one coupler are short-circuited, and those of the other are open-circuited. This creates a +90-degree phase shift in one coupler, and a -90-degree phase shift in the other, resulting in a 180-degree difference between the outputs. The phases of these couplers track well over a wide bandwidth, making the balun very broadband. Figure 4 shows the balun's measured amplitude and phase balance, and Figure 5 shows the loss and the even-order spurious-response suppression provided by the balun. Because it is reasonably compact and entirely planar, this balun is well suited for use in monolithic circuits.

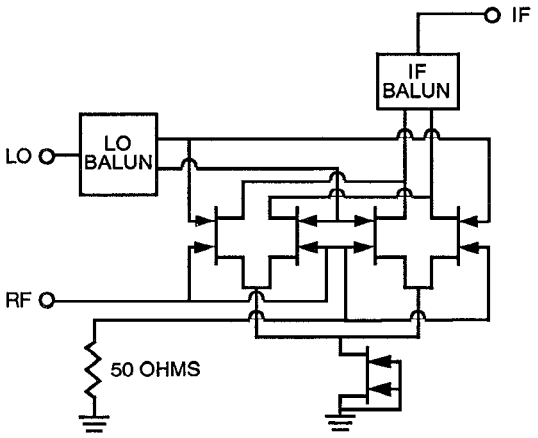

Figure 2. Dual-gate doubly balanced mixer circuit with a current source in series with the sources. This allows the use of a single-ended input from dc to 5 GHz.

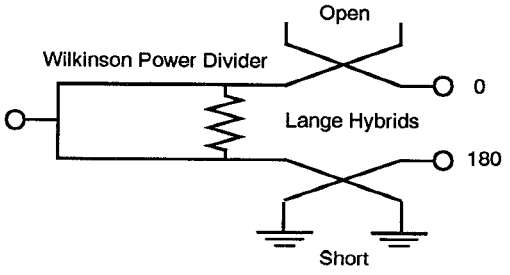

Figure 3. Schematic representation of planar mixer balun

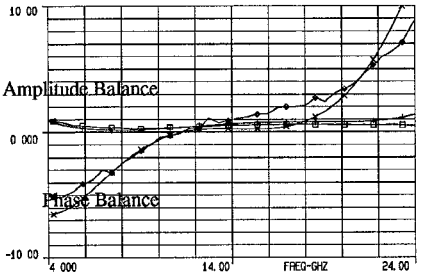

Figure 4. Amplitude balance (dB) and phase balance (degrees) of the planar mixer balun

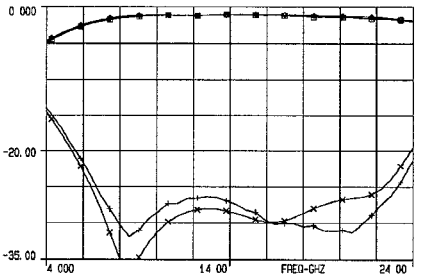

Figure 5. Loss and even-order spurious suppression of the planar mixer balun.

Figure 6 shows a photograph of the mixer. The dual-gate FETs in the mixer were modeled as single-gate devices connected in series; model parameters were obtained by measuring single-gate FETs fabricated on an earlier wafer. Each of the two single-gate FETs that comprise a dual-gate device was modeled in the manner described in [2]. In this model the gate-to-drain I/V characteristic of the FET is modeled by an expression that is designed specifically for accurate intermodulation analysis. The model is most accurate for intermodulation analysis of active mixers and amplifiers.

A comparison of the measured and calculated conversion loss is shown in Figure 7. The third-order, two-tone IM intercept point of the mixer alone (i.e., not including the IF amplifiers) is +15 dBm at the output, with 15 dBm LO power.

3.2 IF and LO Amplifiers

Figure 8 shows a photograph of the IF amplifier. The IF amplifier is a fairly conventional single-stage quadrature-coupled amplifier, using two 600-μm devices. It provides 13 dB narrowband gain at 10 GHz, and has a 27-dBm output IP_3. Its noise figure is 5.5 dB. Figure 9 shows the amplifier's performance, and compares the measured and modeled gain and IP_3. The IP_3 was calculated by means of a commercial harmonic-balance program, with the models described in [2].

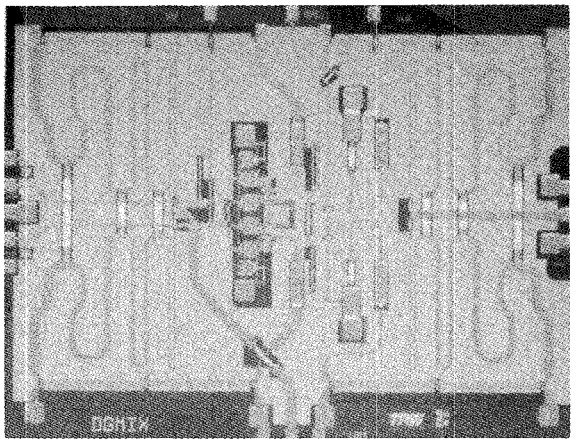

Figure 6. Photograph of the dual-gate doubly-balanced FET mixer with a single-ended RF input.

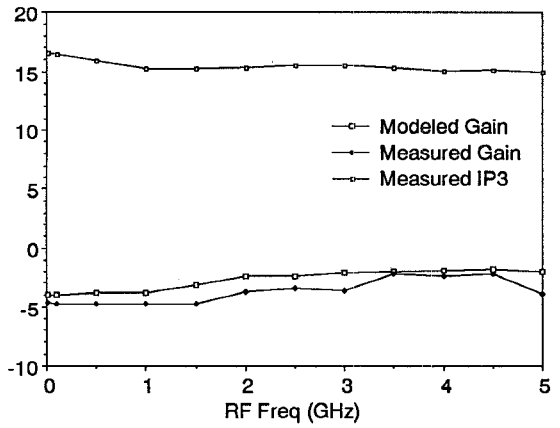

Figure 7. Measured and calculated mixer conversion loss; the IF is fixed. P_{LO} = +15 dBm.

The LO amplifier chain consists of a three-stage parallel-feedback FET amplifier, followed by a single-stage balanced driver amplifier. The three-stage amplifier delivers 15 dB of gain and has a +13-dBm 1-dB compression point. The driver amplifier uses two quadrature-coupled 300 μm MESFETs. Its 1-dB compression point is +16 dBm over the 8-to-16 GHz LO frequency range, and its gain is approximately 6.5 dB. Figure 10 shows a the driver amplifier, and Figure 11 shows its performance.

4.0 Overall Performance

Figure 12 shows a photograph of the MMIC upconverter. The chip dimensions are 8120 μm x 6725 μm. One should note that this circuit was the result of a first-pass design, and no special effort was made to minimize the size of the chip. The circuit in the middle-right side of the chip, labelled IF_SE, is a test circuit, a singe-ended version of the IF amplifier. Figure 13 shows the passband of the complete upconverter, at a fixed IF output frequency. The upconverter exhibits a conversion gain of greater than 6.0 dB over the 5-GHz bandwidth, with 2.0 dB pp gain flatness. Also shown is the output IP_3, which is greater than 23.5 dBm over most of the band, and greater than 22 dBm for the entire band.

Table 1 shows the spurious-response levels of the complete circuit measured at the relatively high input level of -3 dBm. The most important spurious responses are the lower harmonics of the input frequency. The worst of these, the (2, 0) response, is -40 dBc; this corresponds to a second-harmonic intercept point of approximately +45 dBm. Other spurious responses associated with the second harmonic of the input frequency have intercept points above +40 dBm. This high degree of even-order spurious-response rejection is largely due to the high degree of balance in the LO and IF baluns, and the uniformity and low intrinsic spurious-response levels of the doubly balanced dual-gate mixer.

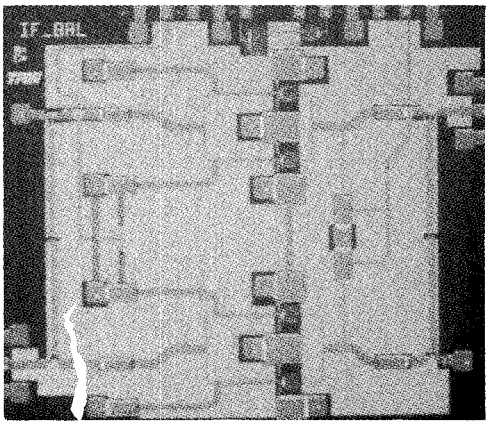

Figure 8. Photograph of the IF amplifier.

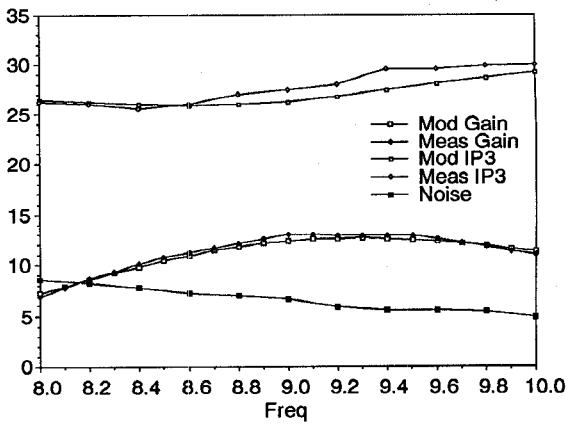

Figure 9. Measured vs. modeled IP3 and gain, and measured noise figure, of the IF amplifier.

Other measured parameters, of the complete downconverter, were as follows:

RF Return Loss	< -20 dB
LO Return Loss	< -12 dB
IF Return Loss	< -15 dB
Noise Figure	< 17 dB (1 to 5 GHz)
LO-to-RF isolation (P_{LO} = 0 dbm)	< -10 dB (.5 to 5 GHz)
LO-to-IF isolation (P_{LO} = 0 dBm)	< -13 dB (.5 to 5 GHz)
DC Power	370 mA @ 5 V

5.0 Yield

The device yields for this very large chip are as follows:

Assumptions:	3 inch wafer DC functionality only
No. of chips per wafer	46
DC Yield	40%
Dicing/Visual Yield	40%
Wafer Yield	85%
No. of chips yielded per wafer	6 (13%)

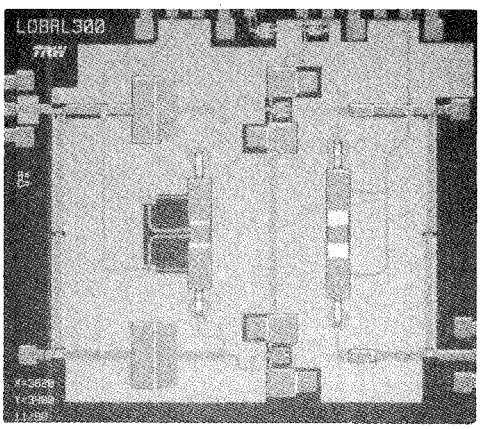

Figure 10. Photograph of 4th stage of the LO amplifier chain

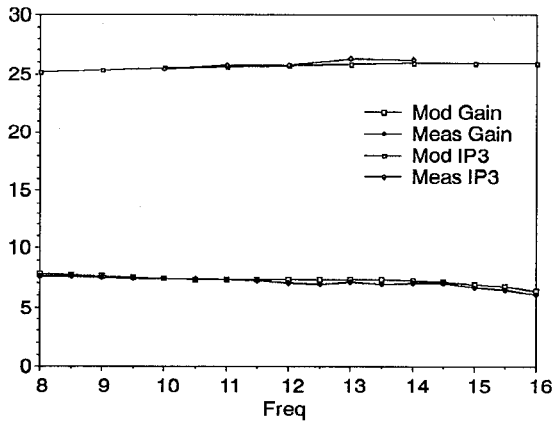

Figure 11. Measured vs. modeled IP3 and gain of the LO amplifier

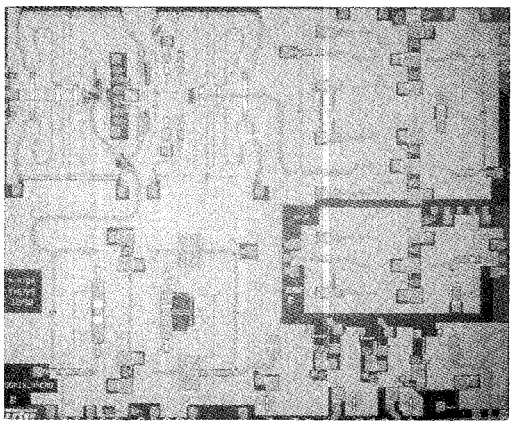

Figure 12. Photograph of complete upconverter. Chip dimensions are 8120 um x 6725 um.

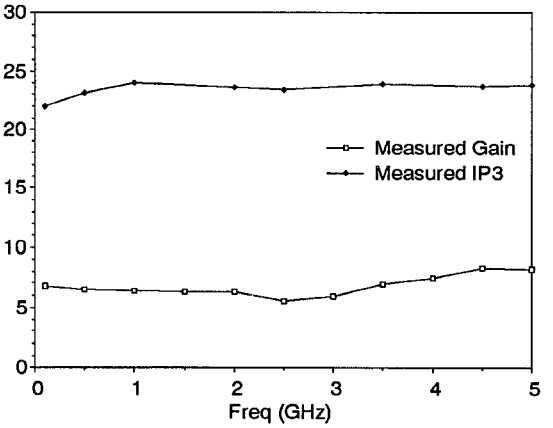

Figure 13. Passband of the complete upconverter.

TABLE 1. Spurious-Response levels (P_{RF} = -3 dBm)

Spurious response: (m,n): m f_{RF} + n f_{LO} = f_{IF}	Output Level, dBc
(1, 0)	25
(2, 0)	40
(3, 0)	60
(4, 0)	75
(5, 0)	90
(-2, 1)	40
(-3, 1)	50
(-4, 1)	82
(-5, 1)	95
(-2, 2)	35
(-3, 2)	58
(-4, 2)	75
(-5, 2)	85

6.0 References

1. S. A. Maas, Microwave Mixers, Artech House, Norwood MA, 1986.
2. S. Maas and D. Neilson, "Modeling MESFETs for Intermodulation Analysis of Mixers and Amplifiers," *IEEE MTT-S Trans. Microwave Theory Tech.*, vol. MTT-38, no. 12 (Dec., 1990).